

660760" F1046E60

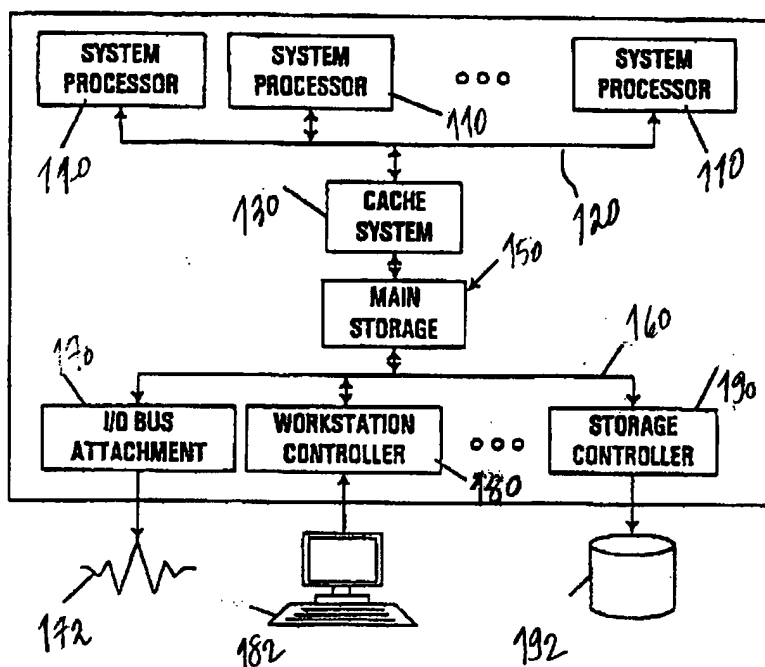


FIG. 1

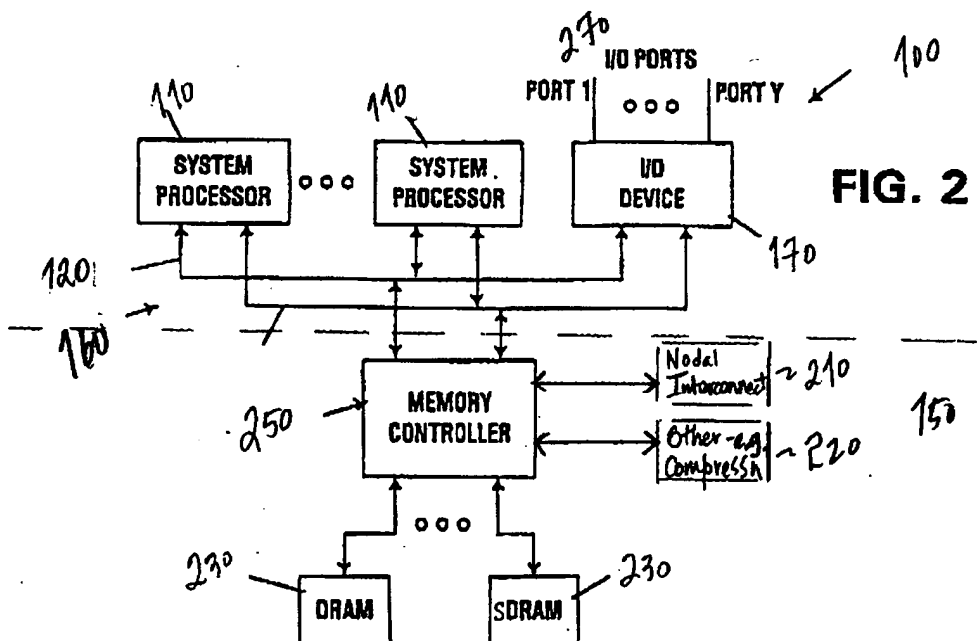
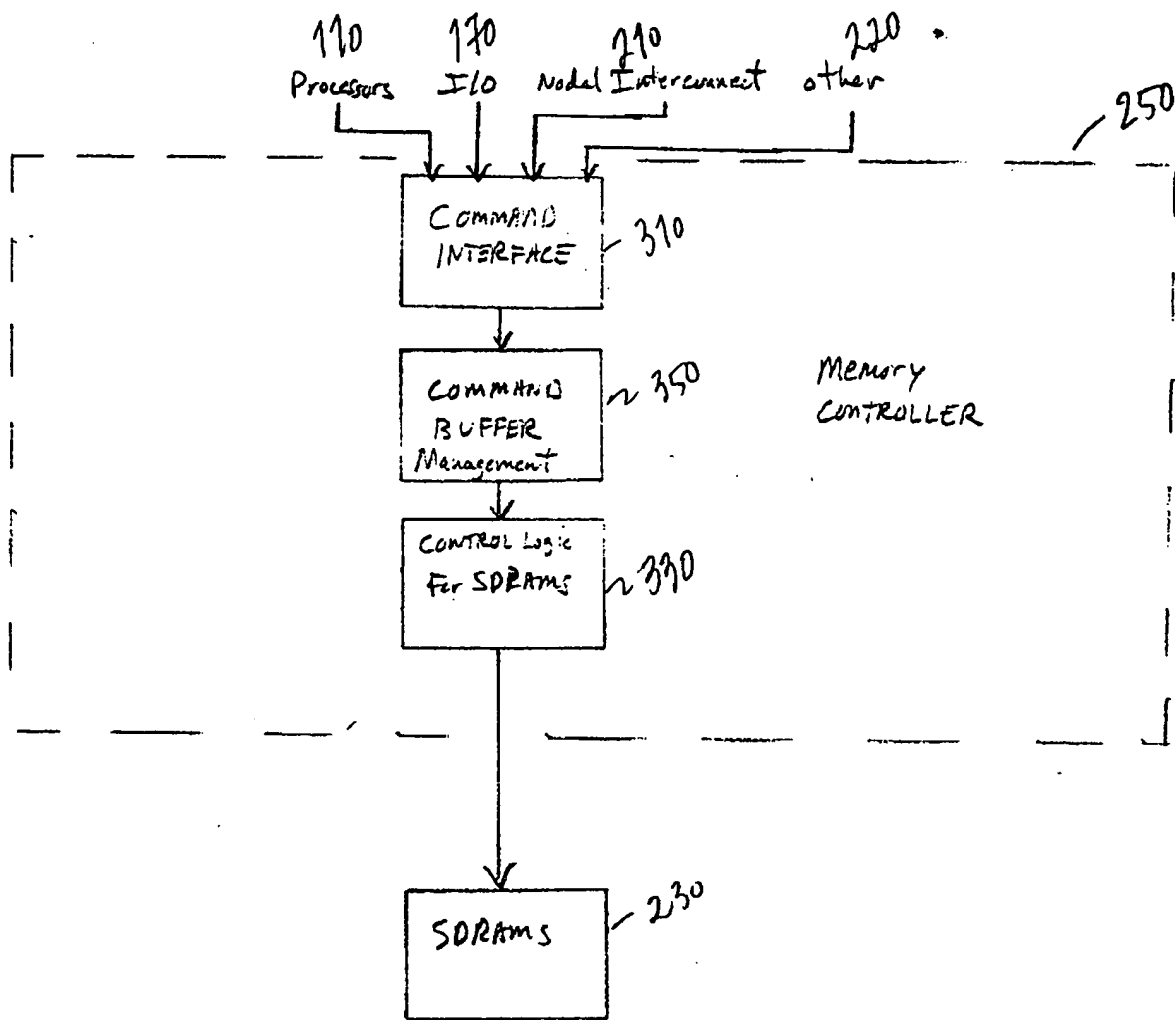


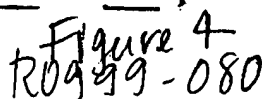
FIG. 2

R0999-080  
Figures 1, 2



650T60" F0H560

RO999-080  
Figure 3



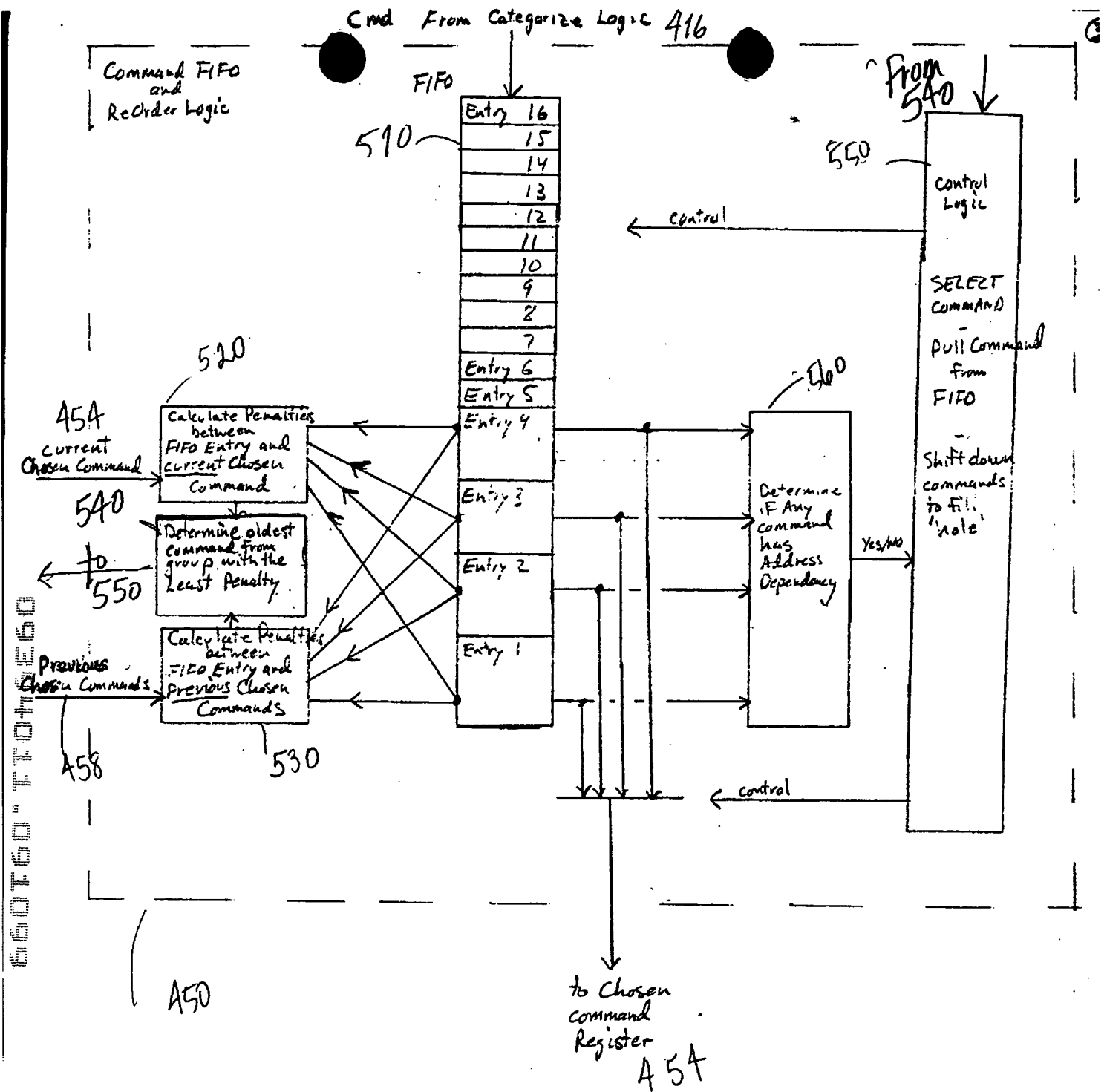


Figure 5  
120999-080

# Command FIFO and Reordering - Flow Diagram

3

660760-104650

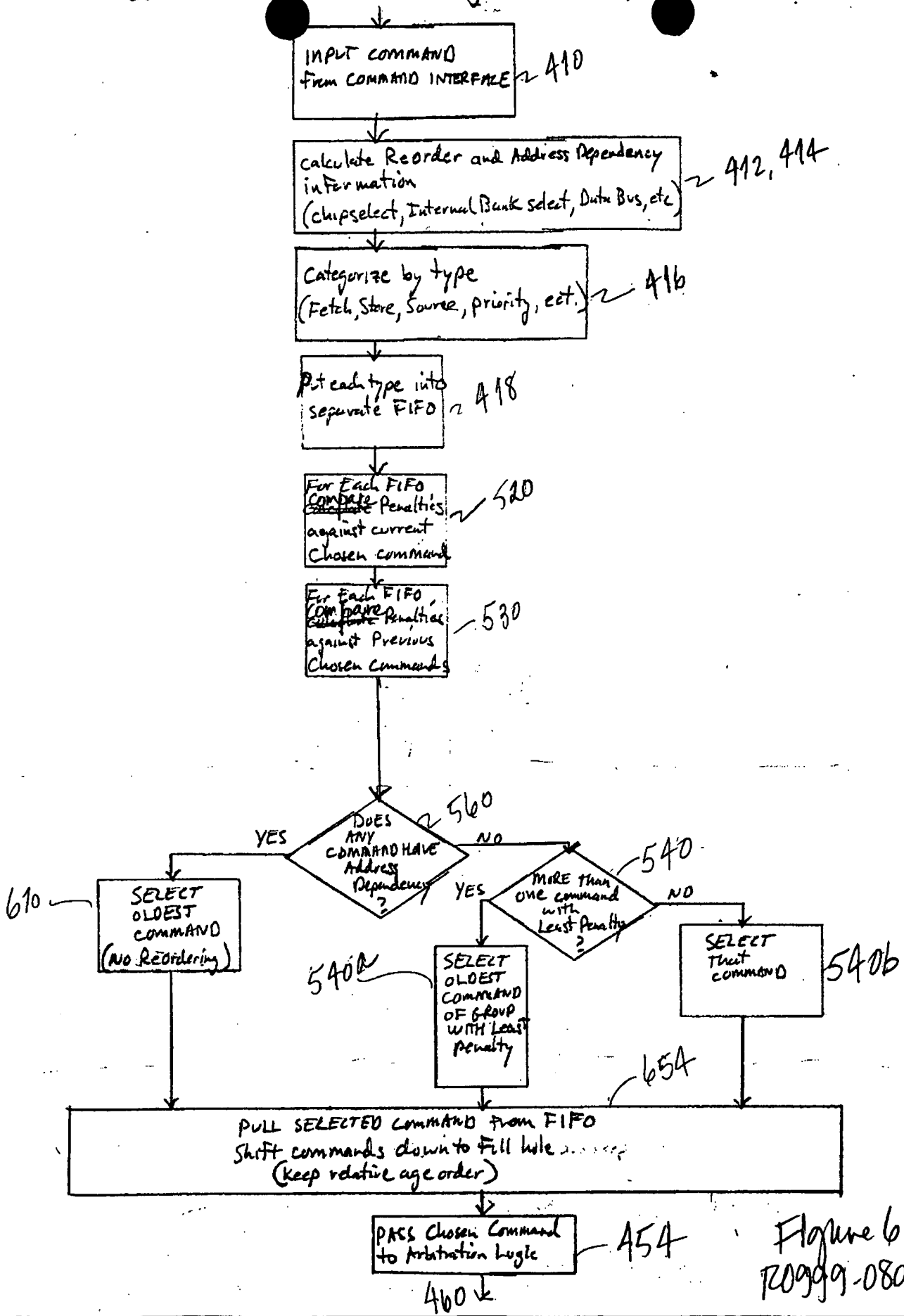


Figure 6  
20999-080

660760-104650

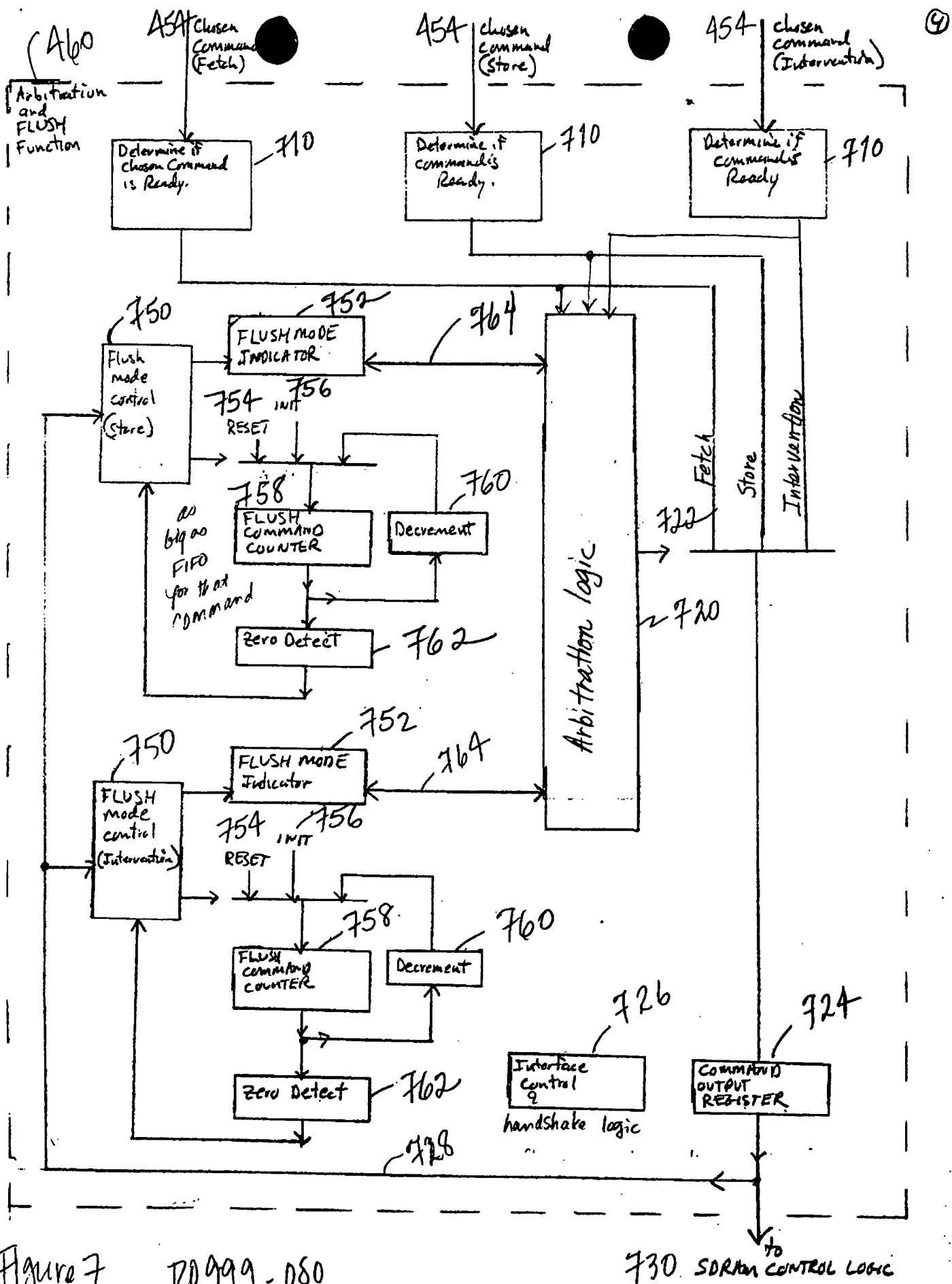
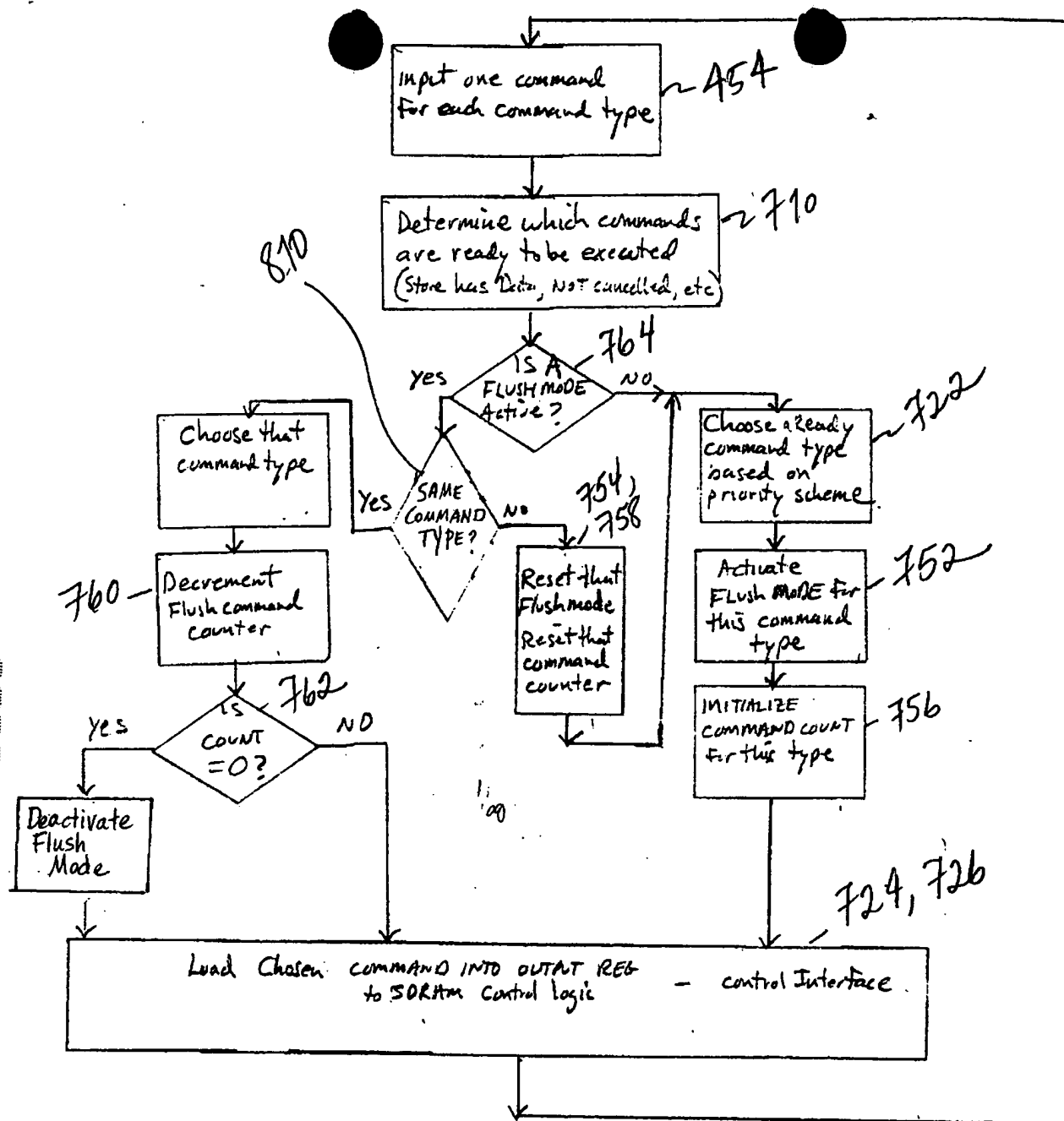


Figure 7 720999-080

730 SDRAM CONTROL LOGIC



FLUSH Function and Arbitrate Logic - Flow Diagram

Figure 8-120999-080

**SECRET**



- COMMAND U address is in same cacheline as command O, and was received after command O.
  - COMMAND M address is in same cacheline as command S, and was received after command S.
- \* IF Commands in both FIFOs, execute in order, then no deadlock.

### Deadlock Condition - (Occured by ReOrdering)



- \* IF certain command chosen by ReOrder Logic, then deadlock  
- Key idea is to not reorder if any command being considered has an address dependency